SCC2698A differences from the SCC2698B AN421

Application Brief by R. L. Mitchell

The SCC2698B Octal UART is an enhanced version of the SCC2698A. The SCC2698B is upwardly compatible from the SCC2698A in its pinout and functionality. The major differences are summarized below:

Product Identitication

The A version is identified on the product marking and on the data sheet's ordering code as SCC2698AC1 xyy; where xyy identifies the package type and pin count (N64 tor 64–plastic DIL and A44 for 84–pin PLCC). The B version is identified as SCC2698Bt1xyy; where xyy identifies the packaging and t identifies the operating temperature range (C for 0° to 70°C and A for –40°C to +85°C). Each device may go through several revisions during its life cycle. The revision is included on the package marking after the lot identification date code and assembly plant. The following is an example of typical product marking:

SCC2698BC1N64 . . . Part number
DU87101 . . . . . Lot identification
8825K– . . . . . Date code (1988 week 25); Assembly plant (K = Korea); Revision Indicator (dash = Non Revision).

The SCC2698A was originally produced as a non–revision product and a dash appeared in the revision position, then it was released as revision A with an A replacing the dash.

Auto–Echo and Remote Loopack Anomaly

The SCC2698A non–revision product contained the following anomaly:

In both Auto–Echo and Remote Loopback channel modes errors may appear in the retransmitted data stream if the baud rate of the received data stream is higher than the baud rate clock on the UART. Errors may also occur if there is jitter in the data bit edge time as may occur in data streams received through a modem. Any amount of baud rate difference or jitter will cause random errors.

Do not rely on the retransmitted data in Auto–Echo or Remote Loopback modes. This anomaly was corrected in the 1. SCC2698A revision A and never appeared in the SCC2698B.

Change-of-State Anomaly

A bug in the change–of-state detector logic of the SCC2698A could cause the occasional miss of a change. The inputs are automatically sampled every 25µs at the standard 3.6864MHz crystal frequency. The miss will occur in the SCC2698A if the flag bits are being read while a new change is being loaded by the sampling circuit. This is corrected on the SCC2698B by preventing new changes from being loaded while a read is occurring.

Register Upate Logic

Several control registers have beer changed from transparent latches to edge–triggered registers to insure that transient conditions on the bus are no longer passed through the registers. The SCC2698A contained complex register update logic which could result in some application problems. This change has permitted the removal of the register update logic. Programs written for the SCC2698A will work with the SCC2698B revision.

The SCC2698A's Register Update Logic attempts to prevent programming errors from affecting part operation. When a write to a control register is performed, it is delayed internally until the receiver(s) and transmitter(s) have completed their current operations. If the update would affect only one channel, then the delay will end when that channel's transmitter and receiver have each completed their current operation and gone idle. If the operation would affect both channels within a block (i.e., change the counter/timer mode) then the delay will not end until both receivers and transmitters have completed their current operations. If a transmitter is being fed a series of bytes it could lock out the update for a long period of time. The registers controlled by the update logic were MR1 MR2 CSR OPCR and ACR. The update logic automatically disables the receiver(s) at the end of the current byte. This update logic could cause the following operation problems:

1. One or both receivers within a block may become disabled (stop functioning) when the function of an I/O pin is changed the mode of the timer counter/timer is changed or any changes are made to the configuration of either receiver or transmitter.

2. Changes to the mode of the counter/timer the mode of the I/O pins or the configuration of either transmitter or receiver may be delayed in taking effect from microseconds to hours later.

In removing this logic for the SCC2698B version the MR1 MR2 CSR OPCR and ACR registers have been made edge–triggered. This change insures that register bits that are written with their previous value will not have their functions affected by the write since transient conditions on the bus are no longer passed through the registers. For previous products such as the SCN2681 we have recommended in AN405 that both the transmitler and receiver be disabled by software while either is being reconfigured to avoid problems caused by transient conditions on the bus. In the SCC2698B it will now only be necessary to disable the function being reconfigured. For example; the CSR registers each contain four bits to control the receive clock and four more bits to control the transmit clock source. With the edge–triggered registers in the SCC2698B, only the transmitter will have to be disabled if only its clock source is being modified.

I/O Enhancemsnts

Sixteen pins, MP12a–h and MP13a–h that were input only on the SCC2698A, may now be programmed to operate as outputs on the SCC2698B by programming OPCR bit 7 to a one. The pins in question are only available on the 84pin PLCC package option and were renamed mulitpurpose pins (MPP1a–h and MPP2a–h) to distinguish them from the input pins. The MP12a–h pins of the SCC2698A are now the MPP1a–h pins of the SCC2698B and the MP13a–h pins have become MPP2a–h. The new outputs provide transmitter ready (TxRDY) and receiver ready (RXRDY) interrupts for each of the channels while still maintaining a Request–To–Send output (RTSN). OPCR(7) which is not used in the SCC2698A should be programmed to zero to maintain software compatibility. There are four OPCRs in the SCC2698 for blocks A through D. Setting bit 7 of a given OPCR will convert both of the MPP1 pins and both of the MPP2 pins per pair of channels into outputs. The enhanced pins become inputs on re–set maintaining compatibility with the SCC2698A. When programming as inputs the MPP1 and MPP2 pins operate as previously to provlde general purpose inputs (GPI), transmit clock inputs (TxC) or receive clock inputs (RxC). As outputs MPP1 provides the transmit holding register empty signal (TxRDY) and MPP2 provides the receiver FIFO not empty/full signal (RxRDY/FFULL). These signals were previously only available on the MPO pin which was often needed for the Request–To–Send.

The MPP1 and MPP2 pins each have a P–channel pull–up resistor to provide a logic 1 when they are left unconnected as inputs. The output driver is an open drain N–channel transrstor.

In summary for the SCC2698B:

OPCR(7) = 0 MPP1x will be a GPI or TCLK input and MPP2x will be a GPI or RCLK input.

OPCR(7) = 1 MPPlx will be a TxRDY output and MPP2x will be a RxRDY/ FFULL output.

Testability

Pin 41 of the 64–pin DIL package was a no connect on the SCC2698A but becomes a test input on the SCC2698B. When using the DIL package neither CSR(7:4) nor CSR(3:O) should be programmed to Hex E or F. These values will cause the “A” version to attempt to use inputs that are not available in the 64-pin package option (MPI2 and MPI3 pins) and will cause the “B” version to use the test pin as an external baud rate clock input common to all channels. Voltages on Pin 41 should not exceed the absolute maximum ratings. This pin may be tied high, tied low or left open.

Literature

The SCC2698A is fully described in the “SCC2698 Octal Universal Asynchronous Receiver/Transmitter” product specification dated July 13, 1987. Later issues of this product specification will be retitled SCC2698A etc. to better distinguish it from the “SCC2698B Enhanced Octal Universal Asynchronous Receiver/Transmitter product specification.

Application Note AN410 was originally written to support the SCC2698A. It has been revised to AN410B and retitled to include the SCC2698B. AN410B can be used for design of both versions of the Octal UART.